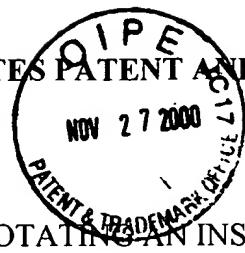


RECEIVED

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant(s): John S. Yates, Jr. et al
 Serial No.: 09/429.094
 Filed: October 28, 1999
 Title: SIDE TABLES ANNOTATING AN INSTRUCTION STREAM



Art Unit: 2824
 Examiner: unassigned

INFORMATION DISCLOSURE STATEMENT

COMMISSIONER FOR PATENTS
 Washington, D.C. 20231

In accordance with 37 C.F.R. §§ 1.56, 1.97 and 1.98, Applicant wishes to make of record the enclosed items, as listed on the accompanying Form PTO-1449. Applicant respectfully requests the Examiner to fully consider the items and independently ascertain their teaching before issuance of the next action, and to make them of record in the file. The Examiner is also requested to initial and return a copy of the enclosed Form PTO-1449 to evidence such consideration.

Of the references listed on the enclosed Form 1449, the following are believed to be the most pertinent:

- U.S. Patent No. 3,781,823, Senese
- U.S. Patent No. 5,307,504, Robinson
- U.S. Patent No. 5,432,795, Robinson
- U.S. Patent No. 5,515,518, Stiles
- U.S. Patent No. 5,664,159, Richter
- PCT publication WO 97/50031, Farber
- Ebciooglu and Altman, IBM Research Report, DAISY: Dynamic Compilation for 100% Architectural Compatibility, IBM Research Division (1996)

The most pertinent portion of the Baxter '602 patent is believed to be Fig. 103, Fig. 110, col. 212, and cols. 345-358, though even that portion of Baxter '602 is only slightly pertinent. The Examiner is requested to independently ascertain the teaching and evaluate the relevance of each item cited on the Form 1449.

For any item listed on the enclosed copy of Form PTO-1449 for which a copy is not already made of record in this application, a copy was previously cited by or submitted to the

I certify that this correspondence, along with any documents referred to therein, is being deposited with the United States Postal Service on November 21, 2000 as First Class Mail in an envelope with sufficient postage addressed to The Commissioner for Patents, Washington D.C. 20231.

11/29/2000 WKORDMA 00000042 09429094

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180.00 DP

Patent and Trademark Office in application Serial No. 09/239,194, filed January 28, 1999, Yates et al., Executing Programs for a First Computer Architecture on a Computer of a Second Architecture, in application Serial No. 09/322,443, filed May 28, 1999, Reese et al., Profiling of Computer Programs Executing in Virtual Memory Systems, or in application Serial No. 09/385,394, filed August 30, 1999, Yates et al., Computer for Executing Two Different Instruction Sets.

This application is one of a group of applications having similar disclosures. The Examiner is requested to be aware of these other applications, both with respect to potential double patenting issues and with respect to prior art that may be discovered in other applications.

Serial No.	Filing Date	Title
09/239,194	1/28/1999	Executing Programs for a First Computer Architecture on a Computer of a Second Architecture
09/322,443	5/28/1999	Profiling of Computer Programs Executing in Virtual Memory Systems
09/330,852	6/11/1999	Profiling Ranges of Execution of a Computer Program
09/332,263	6/11/1999	Profiling Program Execution By Dense Trace Profiling and Statistical Profiling
09/334,530	6/16/1999	Profiling Execution of Computer Programs
09/339,749	6/24/1999	Profiling Program Execution into Registers of a Computer
09/339,797	6/24/1999	Modifying Program Execution Based on Profiling
09/348,317	7/7/1999	Recording Classification of Instructions Executed by a Computer
09/385,394	8/30/1999	Computer For Executing Two Different Instruction Sets
09/425,401	10/22/1999	Profiling Program Execution to Identify Frequently Executed Portions and to Assist Binary Translation
09/426,989	10/26/1999	Table Look-up For Control of Instruction Execution
09/427,168	10/26/1999	Transferring Execution From One Computer Instruction Stream to Another
09/428,850	10/28/1999	Recording I/O Memory References in Program Execution Profile
09/429,377	10/28/1999	Improving Computer Execution by Opportunistic Adaptation
09/432,752	11/3/1999	Detecting Invalidation of Translated Object Code when Source Object Code is Modified
09/432,753	11/3/1999	Safety-Net Paradigm for Managing Two Execution Modes
09/434,198	11/4/1999	Detecting Modification to Computer Memory by a DMA Device
09/434,394	11/4/1999	Detecting Reordered Side-Effects
09/626,325	7/26/2000	Computer with Two Operating Systems
09/666,110	9/20/2000	Computer for Execution of Two Instruction Sets
09/667,226	9/21/2000	Exception Mechanism for a Computer
09/672,424	9/28/2000	Complex Instruction Set Computer
09/672,440	9/28/2000	Managing Instruction Side-Effects
09/672,841	9/28/2000	Validation of Memory References

A number of references are being made of record in these other applications in Information Disclosure Statements being filed contemporaneously herewith. It is believed that none of the references made of record in these other applications are pertinent to the claims of the current

application, except those that are made of record in this application and listed in this Form 1449. Nonetheless, the Examiner is requested to be aware of these additional applications and items made of record therein.

Recent commercial efforts in the general field have included projects at NexGen and Exponential Technology, Inc. It is not believed that the capabilities of any of these prior computers relate to the inventions claimed in this application; nonetheless, the examiner's attention is drawn to these machines as possibly relevant prior art.

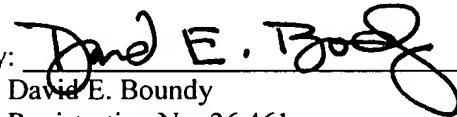
A check in the amount of \$ 180.00 is enclosed in payment of the fee due under C.F.R. §1.17(i)(1).

The Commissioner is hereby authorized to charge any additional fees that may be required for this Information Disclosure Statement, or credit any overpayment, to Deposit Account 50-0324, Order No. 30585/16.

Respectfully submitted,

SHEARMAN & STERLING

Dated: November 21, 2000

By: 
David E. Boundy
Registration No. 36,461

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